SPECIFICATION

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APPARATUS FOR REDUCING SOFT ERRORS IN DYNAMIC CIRCUITS

Background of the Invention

[0001] The present invention relates to the field of integrated circuits; more specifically, it relates to reducing soft errors in integrated circuits that include dynamic circuits. BACKGROUND OF THE INVENTION Dynamic circuits, such as domino circuits, for example, are widely used in high-speed integrated circuit designs. This is because dynamic circuits typically provide area and speed advantages over corresponding static complementary metal oxide semiconductor (CMOS) circuits.

[0002] Dynamic circuits, however, are more vulnerable to soft errors as compared to their static counterparts. A soft error is a transient, single event upset that changes the state of a circuit node or other internal storage element. Soft errors, for example, may be caused by alpha particles or cosmic rays impinging on the integrated circuit device.

[0003] Alpha particles are charged particles that may originate from the decay of trace impurities in integrated circuit packaging materials, for example. Cosmic rays may include heavy ions and protons that, either directly or indirectly, may have an ionization effect within the integrated circuit device semiconductor material. In either case, the charged particles from these sources may change the charge at an integrated circuit node such that the node actually transitions to an opposite logical state.

[0004] The critical charge (Qcrit) at a node is an indication of the susceptibility of the node to such soft errors. Qcrit is the minimum charge beyond which operation of a circuit will be affected. Thus, if an ion strike causes charge collected at a node to

exceed Qcrit, the node may erroneously transition from a logical one state to a logical zero state, or from a logical 0 to a logical 1 state.

[0005] Since the maximum frequency at which an integrated circuit can be clocked depends on the Qcrit of the circuit, the immunity of the circuit must be traded off against the clock frequency. Clock frequency is adversely effected by higher Qcrit levels in dynamic circuits. The same integrated circuit may be used in multiple applications. High performance applications require high clock frequencies and thus a lower Qcrit. High reliability applications require high Qcrit, but must run at lower clock frequencies. A given device may be used in either application. A single device may be used in a high reliability mode at one moment and in a high performance mode another moment.

[0006] Therefore, the tradeoff between reliability against soft errors expressed as a Qcrit level and performance of a dynamic circuits presents designers of dynamic circuits significant problems.

Brief Summary of the Invention

[0007] A first aspect of the present invention is an integrated circuit comprising: a dynamic logic gate having an output node at which a logical output value of the logic gate is detected; and selectable circuit means for alteration of the soft error susceptibility of the dynamic logic gate.

[0008] A second aspect of the present invention is an integrated circuit comprising: a dynamic logic gate having an output node at which a logical output value of the logic gate is detected; and a keeper circuit adapted to selectively alter the critical charge of the dynamic logic gate.

[0009] A third aspect of the present invention is an integrated circuit comprising: a dynamic logic gate having an output node at which a logical output value of the logic gate is detected; a keeper circuit providing a level of critical charge to the output node; and a body bias circuit, the body bias circuit adapted to selectively alter the bias voltage applied to the bodies of input devices of the dynamic logic gate.

Brief Description of the Several Views of the Drawings

[0010] The features of the invention are set forth in the appended claims. The invention itself, however, will be best understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

[0011] FIG. 1 is a schematic diagram of a dynamic circuit;

[0012] FIG. 2 is a schematic diagram of a dynamic circuit according to a first embodiment of the present invention;

[0013] FIG. 3 is a schematic diagram of a dynamic circuit according to a second embodiment of the present invention; and

[0014] FIG. 4 is a schematic diagram of a dynamic circuit according to a third embodiment of the present invention.

Detailed Description of the Invention

[0015] Critical charge is defined as the minimum amount of charge injected into a given circuit node which is sufficient to corrupt the logic state of the circuit. Corruption of the logic state of the circuit is defined as changing the state of the internal node and/or the output of the circuit from a logical 0 before the radiation event to a logical 1 after the radiation event or from a logical 1 before the radiation event to a logical 0 after the radiation event. The injection of this charge into a circuit node is presumed in this definition to be caused by a radiation-induced ionization incident occurring on the given node.

[0016] FIG. 1 is a schematic diagram of a dynamic circuit. In FIG. 1, dynamic circuit 100 includes a dynamic logic gate 105 having inputs PC, A, B, and C and a precharge/output node PCN and a keeper circuit 110 having an output Z. An input of keeper circuit 110 is coupled to precharge/output node PCN of dynamic logic gate 105.

[0017] Dynamic logic gate 105 is a three input domino NAND gate and is used as an exemplary dynamic logic gate. Other types of domino gates or other combinational logic gates may be substituted. Dynamic logic gate 105 includes a precharge device (PFET T1), and NFETs T2, T3, T4 and T5. NFET T5 is a foot switch. The source of PFET

T1 is coupled to VDD, the gate of PFET T1 is coupled to input PC and the drain of PFET T1 is coupled to the drain of NFET T2. The gate of NFET T2 is coupled to input A and the source of NFET T2 is coupled to the drain of NFET T3. The gate of NFET T3 is coupled to input B and the source of NFET T3 is coupled to the drain of NFET T4. The gate of NFET T4 is coupled to input C and the source of NFET T4 is coupled to the drain of NFET T5. The source of NFET T5 is coupled to ground and the gate of NFET T5 is coupled to input PC. Input PC receives a precharge signal that charges precharge/output node PCN prior to data signals being applied to inputs A, B and C. During a precharge phase precharge/output node PCN may be charged to a pre-determined level (a logical 1 in the present example) and during an evaluate phase, an output value based on data signals applied to input nodes A, B and C may be read out at output Z.

[0018] Keeper circuit 110 includes a keeper device (PFET T6) and an inverter I1. The drain of PFET T6 and the input of inverter I1 are coupled to precharge/output node PCN. The output of inverter I1 is coupled to output Z. The gate of PFET T6 is coupled between the output of inverter I1 and output Z. The source of PFET T6 is coupled to VDD. Inverter I1 acts as a feedback device for PFET T6. Because the charge on precharge/output node PCN is not held by any device (it is dynamic), keeper circuit 110 keeps precharge/output node PCN charged through PFET T6. A logical 1 (the precharge state) on precharge/output node PCN turns on PFET T6 so precharge/output node PCN is coupled to VDD. During evaluate mode whenever a logical 1 is on precharge/output node PCN, PFET T6 is off.

[0019] Charge can be lost to precharge/output node PCN through various leakage paths, by capacitive coupling of precharge/output node PCN , by spilling charge through junction diodes and by a radiation event affecting devices coupled to precharge/output node PCN. By design, PFET T6 can only supply a trickle of positive charge to precharge/output node PCN, otherwise PFET T6 could override the output signal generated by the data signals at inputs A, B and C or add a hysteric delay. The problem with a discharge of precharge/output node PCN caused by a large radiation event during precharge mode is that PFET T6 cannot charge precharge/output node PCN back quickly and the circuit(s) coupled to output Z interprets the discharge as a true data signal;, thus a soft error is generated. For example, with a logical 0 on input

A and logical 1 on inputs B and C, a negative radiation event in bulk silicon substrates or a positive radiation event in silicon-on-insulator (SOI) substrates event to the gate (or other devices) device coupled to input A will cause precharge/output node PCN to discharge.

[0020] FIG. 2 is a schematic diagram of a dynamic circuit according to a first embodiment of the present invention. In FIG. 2, dynamic circuit 200 includes a dynamic logic gate 205 having inputs PC, A, B, and C and a precharge/output node PCN and a keeper circuit 210 having an output Z. An input of keeper circuit 210 is coupled to precharge/output node PCN of dynamic logic gate 205.

[0021] Dynamic logic gate 205 is a three input domino NAND gate and is used as an exemplary dynamic logic gate. Other types of domino gates or other combinational logic gates may be substituted. Dynamic logic gate 205 includes PFET T7, and NFETs T8, T9, T10 and T11. Dynamic logic gate 205 is a duplicate of dynamic logic gate 105 illustrated in FIG. 1 and described supra, wherein PFET T7, and NFETs T8, T9, T10 and T11 of dynamic logic gate 205 correspond respectively to PFET T1, and NFETs T2, T3, T4 and T5 of dynamic logic gate 105.

[0022] Keeper circuit 210 includes a first keeper device (PFET T12) an inverter I2. The drain of PFET T12 and the input of inverter I2 are coupled to precharge/output node PCN. The output of inverter I2 is coupled to output Z. The gate of PFET T12 is coupled between the output of inverter I2 and output Z. The source of PFET T12 is coupled to VDD. Keeper circuit 210 further includes an immunity gating device (PFET T14), a second keeper device (PFET T13) and a register 215. The drain of PFET T13 is coupled to precharge/output node PCN, the source of PFET T13 is coupled to the drain of PFET T14, and the gate of PFET T13 is coupled to the gate of PFET T12. The source of PFET T14 is coupled to VDD and the gate of PFET T14 is coupled to register 215. PFET T13 and PFET T12 are capable of supplying only a trickle of positive charge. The amount of charge PFETs T12 and T13 can supply may be the same or PFET T13 may supply more or less charge than PFET T12.

[0023] Register 215 contains a bit register storing an enable-enhanced immunity bit (EI) and necessary circuitry to drive an EI signal to the gate of PFET T14. When the EI signal is a logical 0, enhanced immunity is enabled and when the EI bit is a logical 1,

enhanced immunity is disabled.

[0024] A logical 0 (the precharge state) on precharge/output node PCN turns on PFETs T12 and T13 so precharge/output node PCN is coupled to VDD. Since PFET T12 is coupled directly to VDD, PFET T12 supplies charge to precharge/output node PCN whenever dynamic circuit 200 is in precharge mode. However, PFET T13 is gated by PFET T14, and can only supply charge to precharge/output node PCN when the EI signal is a logical 0 (enhanced immunity enabled). During evaluate mode both PFETs T12 and T13 are off. In enhanced immunity mode, Qcrit is increased, so the clock frequency of dynamic circuit 200 may need to be decreased.

[0025] While only two keeper devices are illustrated in FIG. 2, a third keeper device responding to a second EI bit may be added, and there is no limit to the number of additional keeper devices responding to corresponding EI bits that may be added.

[0026] FIG. 3 is a schematic diagram of a dynamic circuit according to a second embodiment of the present invention. In FIG. 3, dynamic circuit 300 includes a dynamic logic gate 305 having inputs PC, A, B, and C and a precharge/output node PCN and a keeper circuit 310 having an output Z. An input of keeper circuit 310 is coupled to precharge/output node PCN of dynamic logic gate 305. Dynamic circuit 300 further includes a body bias circuit 315 coupled to dynamic logic circuit 305 as described infra.

[0027] Dynamic logic gate 305 is a three input domino NAND gate and is used as an exemplary dynamic logic gate. Other types of domino gates or other combinational logic gates may be substituted. Dynamic logic gate 305 includes PFET T15, and NFETs T16, T17, T18 and T19. Dynamic logic gate 305 is a similar to gate 105 illustrated in FIG. 1 and described supra, wherein PFET T15, and NFETs T16, T179, T18 and T19 of dynamic logic gate 305 correspond respectively to PFET T1, and NFETs T2, T3, T4 and T5 of dynamic logic gate 105. The differences being coupling of the bodies of NFETs T16, T17 and T18 as described infra.

[0028]

Keeper circuit 310 includes a keeper device (PFET T20) an inverter I3. The drain of PFET T20 and the input of inverter I3 are coupled to precharge/output node PCN. The output of inverter I3 is coupled to output Z. The gate of PFET T20 is coupled between

the output of inverter I3 and output Z. The source of PFET T20 is coupled to VDD. Keeper circuit 310 functions identically to keeper circuit 110 illustrated in FIG. 1 and describes supra.

[0029] Body bias circuit 315 includes a multiplexer 320 and a register 325. A first input of multiplexer 320 is coupled to a positive bias voltage and a second input of multiplexer 320 is coupled to ground. The output of multiplexer 320 is coupled to each body of NFETs T16, T17 and T18 of dynamic logic gate 305. Register 325 is coupled to the control input of multiplexer 320.

[0030] Register 325 contains a bit register storing an enable-enhanced immunity (EI) bit and necessary circuitry to drive an EI signal to the control input of multiplexer 320. When the EI signal is a logical 0, enhanced immunity is enabled and ground is applied to the bodies of NFETs T16, T17 and T18. When the EI bit is a logical 1, enhanced immunity is disabled and bias voltage is supplied to the bodies of NFETs T16, T17 and T18.

[0031] Independent body bias is easily applied to devices fabricated in SOI substrates. In bulk silicon applying substrate bias is equivalent. In the case of a bulk silicon substrate, NFETs T16, T17 and T18 are fabricated in a P-well isolated from other devices. Body bias circuit 320 would then be coupled to the P-well. In operation, body bias is applied static, that is when dynamic circuit 300 is operated. Applying a positive bias voltage (enhanced immunity not enabled) to the bodies of NFETs T16, T17 and T18 decreases the threshold voltage (V_T) of those devices. Applying ground (enhanced immunity enabled) to the bodies of NFETs T16, T17 and T18 increases the threshold voltage (V_T) of those devices. Increasing the threshold of NFETs T16, T17 and T18 makes NFETs T16, T17 and T18 harder to turn on and thus increases immunity to radiation events.

[0032] While the same bias was described as being applied to bodies of all domino input NFETs, it is possible to apply a first bias to a first set of input NFETs, a second bias to a second set of input NFETs and so on by adding additional multiplexer's responding to corresponding additional EI bits.

[0033] FIG. 4 is a schematic diagram of a dynamic circuit according to a third

embodiment of the present invention. In FIG. 4, dynamic circuit 400 includes a dynamic logic gate 405 having inputs PC, A, B, and C and a precharge/output node PCN and a keeper circuit 210 having an output Z. An input of keeper circuit 410 is coupled to precharge/output node PCN of dynamic logic gate 405.

[0034] Dynamic logic gate 405 is a three input domino NAND gate and is used as an exemplary dynamic logic gate. Other types of domino gates or other combinational logic gates may be substituted. Dynamic logic gate 405 includes PFET T21, and NFETs T22, T23, T24 and T25. Dynamic logic gate 405 is similar to dynamic logic gate 105 illustrated in FIG. 1 and described supra, wherein PFET T21, and NFETs T22, T23, T24 and T25 of dynamic logic gate 205 correspond respectively to PFET T1, and NFETs T2, T3, T4 and T5 of dynamic logic gate 105. The difference is the gate of PFET T21 is coupled to a VDD source in keeper circuit 410 as described infra.

[0035] Keeper circuit 410 includes a keeper device (PFET T26) an inverter I4, a first multiplexer 415, a second multiplexer 420, and a register 425. The drain of PFET T26 and the input of inverter I4 are coupled to precharge/output node PCN. The output of inverter I4 is coupled to output Z. The gate of PFET T26 is coupled between the output of inverter I4 and output Z. The source of PFET T26 is coupled to an output of second multiplexer 420. PFET T26 functions similarly to PFET T6 of dynamic circuit 100 illustrated in FIG. 1 and described supra, except that PFET T26 charges precharge/output node PCN with a selectable voltage as described infra. A first input of first multiplexer 415 is coupled to VDD1 and a second input of first multiplexer 415 is coupled to VDD2. A first input of second multiplexer 420 is coupled to VDD1 and a second input of second multiplexer 420 is coupled to VDD2. VDD1 is greater than VDD2.

[0036] Register 425 contains a bit register storing an enable-enhanced immunity (EI) bit and necessary circuitry to drive an EI signal to control inputs of first and second multiplexer's 415 and 420. When the EI signal is a logical 0, enhanced immunity is enabled and PFET T26 is coupled to VDD1. When the EI bit is a logical 1, enhanced immunity is disabled and PFET T26 is coupled to VDD2.

[0037] Similarly, PFET T21 (the precharge device of dynamic logic gate 405) is coupled to an output of first multiplexer 415. When the EI signal is a logical 0, enhanced

immunity is enabled and PFET T21 is coupled to VDD1 thus precharging precharge/output node PCN to VDD1. When the EI bit is a logical 1, enhanced immunity is disabled and PFET T26 is coupled to VDD2 thus precharging precharge/output node PCN to VDD2.

[0038] The higher the supply voltage to dynamic logic gate 405, the more resistant dynamic logic gate 405 is to radiation events. The supply voltage to dynamic logic gate 405 via PFET T21 and the keeper voltage applied to precharge/output node PCN may thus be increased dynamically when increased soft error rate immunity is desired or statically for applications requiring increased soft error rate immunity.

[0039] There are two modes of operation for dynamic gate circuits 200, 300 and 400. The EI bit may be fixed when the integrated circuit chip is fabricated or may be changed dynamically as the Qcrit required of dynamic gate circuits 200, 300 and 400 change over time.

[0040] While two multiplexer's are illustrated in FIG. 4, a single multiplexer coupled to both PFETs T21 and T26 may be used. And while only voltage sources, VDD1 and VDD2, are illustrated in FIG. 4, three or more supply voltages, each corresponding to an additional EI bit may be added.

[0041] All three embodiments of the present invention may be applied to both silicon and SOI devices.

[0042] Thus, the present invention provides a method to set the Qcrit level of a dynamic circuit as a function of the soft error immunity level of the application for which the dynamic circuit is being used.

[0043] The description of the embodiments of the present invention is given above for the understanding of the present invention. It will be understood that the invention is not limited to the particular embodiments described herein, but is capable of various modifications, rearrangements and substitutions as will now become apparent to those skilled in the art without departing from the scope of the invention. For example, the multiplexer's of various embodiments of the present invention may be replaced by other switching circuits, and the registers of the various embodiments may be replaced with circuits other than registers capable supplying enabling signals.

Therefore, it is intended that the following claims cover all such modifications and changes as fall within the true spirit and scope of the invention.